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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/046,566	10/19/2001	Felix Chow	388682000900	1782

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EXAMINER	
FOX, JAMAL A	

ART UNIT	PAPER NUMBER
2664	

DATE MAILED: 08/10/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/046,566	CHOW, FELIX	
	Examiner	Art Unit	
	Jamal A. Fox	2664	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *19 October 2001*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-36* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☒ Claim(s) *1-15* is/are allowed.

6)☒ Claim(s) *16-22,25-28 and 31-36* is/are rejected.

7)☒ Claim(s) *23,24,29,30 and 33* is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *19 October 2001* is/are: a)☐ accepted or b)☒ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Drawings

1. New corrected drawings in compliance with 37 CFR 1.121(d) are required in this application because the text is illegible (reference characters, sheet numbers, and view numbers must be plain and legible). Applicant is advised to employ the services of a competent patent draftsperson outside the Office, as the U.S. Patent and Trademark Office no longer prepares new drawings. The corrected drawings are required in reply to the Office action to avoid abandonment of the application. The requirement for corrected drawings will not be held in abeyance.

Claim Objections

2. Claim 33 is objected to because of the following informalities: Claim 33, line 1, after "comprises", "means" is spelled incorrectly. Appropriate correction is required.

Claim Rejections - 35 USC § 102

3. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (e) the invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.

4. Claims 16-22, 25-28 and 31-36 are rejected under 35 U.S.C. 102(e) as being anticipated by Yu (U.S. Patent Application Pub. No. 2001/0012288).

Referring to claim 16, Yu discloses a system for parallel (parallel, [0062]) processing bit-synchronous data, wherein a new plurality of bits is shifted in and an old plurality of bits is shifted out of said shift register (shift register, Figures 9A and 9B and respective portions of the spec.) during successive clock cycles (clock cycle, [0143]); and

a de-framer unit (de-framer, [0081] and Fig. 6 ref. sign 11 and Fig. 7 ref. sign 27 and respective portions of the spec.), coupled to said shift register, for detecting (detected, [0092]) valid payload data, wherein said de-framer unit processes in parallel (parallel, [0021] and [0062]) a plurality of bits within said shift register (shift register, Figures 9A and 9B and respective portions of the spec.) during first clock cycle (clock cycle, [0227] and [0279]).

Referring to claim 17, Yu discloses the system of claim 16 wherein said de-framing unit further processes in parallel (parallel, [0021] and [0062]) said plurality of bits within said shift register (shift register, Figures 9A and 9B and respective portions of the spec.) to detect a specified sequence of bits during said first clock cycle (clock cycle, [0227] and [0279]).

Referring to claim 18, Yu discloses the system of claim 17 wherein said de-framing unit searches (searched, [0123]) for a start (start, [0088]) sequence within said shift register wherein said valid payload data bits comprise at least some bits received after said start (start, [0088]) sequence.

Referring to claim 19, Yu discloses the system of claim 18 wherein said de-framing unit further searches (searched, [0123]) for an end (ending, [0056], [0057], [0107], and [0161]) sequence within said shift register (shift register, Figures 9A and 9B and respective portions of the spec.), after said start (start, [0056], [0057], [0107] and [0161]) sequence has been detected, during at least one clock cycle subsequent to said first clock cycle (clock cycle, [0227] and [0279]), wherein said valid payload data bits comprise at least some bits received between said start (start, [0088]) and end sequences.

Referring to claim 20, Yu discloses the system of claim 16, wherein:

said bit-synchronous data comprises bit-synchronous HDLC (HDLC, [0008], [0019], [0080]) data;

said shift register (shift register, Figures 9A and 9B and respective portions of the spec.) stores at least two bytes (two byte, [0166], [0338], [0360]) of said bit-synchronous HDLC (HDLC, [0008], [0019] and [0080]) data;

said new and old plurality of bits each comprise one byte (one byte, [0109]) of data;

said de-framer (de-framer, [0081] and Fig. 6 ref. sign 11 and Fig. 7 ref. sign 27 and respective portions of the spec.) unit comprises a plurality of comparators wherein each comparator is coupled to a unique subset of eight successive bits contained within said shift register;

said start sequence comprises a SOF (start, [0056], [0057], [0107] and [0161]) sequence;

said end sequence comprises a EOF (ending, [0056], [0057], [0107] and [0161]) sequence;

said valid payload data (payload data, [0123] and [0327]) bits comprise at least some bits received between said SOF and EOF sequences (sequence, 0056], [0057], [0107] and [0161]).

Referring to claim 21, Yu discloses the system of claim 20 wherein said de-framer unit further processes in parallel (parallel, [0062]) a plurality of bits stored in said shift register to detect an Abort (abort, [0115] and [0134]) sequence during at least one clock cycle subsequent to said first clock cycle (clock cycle, [0227] and [0279]), wherein if said Abort (abort, [0115] and [0134]) sequence is detected, all bits received after said SOF (start, [0056], [0057], [0107] and [0161]) sequence are discarded (discard, [0139]) and a search for a new SOF (start, [0056], [0057], [0107] and [0161]) sequence is initiated.

Referring to claim 22, Yu discloses the system of claim 20 wherein said de-framer unit further processes in parallel (parallel, [0062]) a plurality of bits within said shift register to detect at least one stuff (stuff, [0299] and [0300]) bit and discards (discard, [0139]) said at least one stuff (stuff, [0299] and [0300]) bit, if detected, wherein said valid payload data (payload data, [0123] and [0327]) bits comprise all bits shifted into said shift register between said SOF (start, [0056], [0057], [0107] and [0161]) sequence and said EOF (ending, [0056], [0057], [0107] and [0161]) sequence, excluding said at least one stuff (stuff, [0299] and [0300]) bit.

Referring to claim 25, Yu discloses a bit-synchronous HDLC engine, comprising:

a shift register (shift register, Figures 9A and 9B and respective portions of the spec.) for storing at least two bytes (two byte, [0166], [0338], [0360]) of bit-synchronous HDLC data, wherein a new byte is shifted in and an old byte is shifted out of said shift register during each successive clock cycle (clock cycle, [0143]); and

a de-framer unit (de-framer, [0081] and Fig. 6 ref. sign 11 and Fig. 7 ref. sign 27 and respective portions of the spec.), coupled to said shift register, for detecting (detected, [0092]) valid payload data (payload data, [0123] and [0327]) within said shift register, wherein said de-framer unit comprises a plurality of comparators (comparing [0027] and [0031]) for detecting a specified sequence of bits within said shift register during a first clock cycle (clock cycle, [0227] and [0279]), wherein each comparator (comparing [0027] and [0031]) is coupled to a unique subset of eight successive bits contained within said shift register (shift register, Figures 9A and 9B and respective portions of the spec.).

Referring to claim 26, Yu discloses the bit-synchronous HDLC engine of claim 25 wherein said de-framer unit detects a SOF sequence during said first clock cycle (clock cycle, [0227] and [0279]) and detects an EOF (ending, [0056], [0057], [0107] and [0161]) sequence during a subsequent clock cycle, wherein said valid payload data (payload data, [0123] and [0327]) comprises at least some of the bits received between said SOF (start, [0056], [0057], [0107] and [0161]) sequence and said EOF (ending, [0056], [0057], [0107] and [0161]) sequence.

Referring to claim 27, Yu discloses the bit-synchronous HDLC engine of claim 26 wherein said de-framer unit further processes in parallel (parallel, [0062]) a plurality of

bits stored in said shift register to detect an Abort (abort, [0115] and [0134]) sequence during at least one clock cycle subsequent to said first clock cycle (clock cycle, [0227] and [0279]), wherein if said Abort (abort, [0115] and [0134]) sequence is detected, all bits received after said SOF (start, [0056], [0057], [0107] and [0161]) sequence are discarded (discard, [0139]) and a search for a new SOF sequence is initiated.

Referring to claim 28, Yu discloses the bit-synchronous HDLC engine of claim 26 wherein said de-framer unit further processes in parallel (parallel, [0062]) a plurality of bits within said shift register to detect at least one stuff bit and discards (discard, [0139]) said at least one stuff (stuff, [0299] and [0300]) bit, if detected, wherein said valid payload data (payload data, [0123] and [0327]) bits comprise all bits shifted into said shift register between said SOF sequence and said EOF (ending, [0056], [0057], [0107] and [0161]) sequence, excluding said at least one stuff bit.

Referring to claim 31, Yu discloses a system for parallel (parallel, [0062]) processing bit-synchronous data, comprising:

means (shift register, Figures 9A and 9B and respective portions of the spec.) for storing a plurality of bits of bit-synchronous data, wherein a new plurality of bits is stored and an old plurality of bits is expelled out of said means for storing during successive clock cycles (clock cycle, [0143]); and

de-framer means (de-framer, [0081] and Fig. 6 ref. sign 11 and Fig. 7 ref. sign 27 and respective portions of the spec.), coupled to said means for storing, for detecting (detected, [0092]) valid payload data and for processing in parallel (parallel, [0021] and

[0062]) a plurality of bits within said means for storing during a first clock cycle (clock cycle, [0227] and [0279]).

Referring to claim 32, Yu discloses the system of claim 31 further comprising means for processing in parallel (parallel, [0021] and [0062]) said plurality of bits within said means for storing to detect a specified sequence of bits during said first clock cycle (clock cycle, [0227] and [0279]).

Referring to claim 33, Yu discloses the system of claim 32 wherein said means for processing in parallel (parallel, [0062]) comprises means for detecting (detected, [0092]) a start (start, [0088]) sequence contained within said means for storing, wherein said valid payload data (payload data, [0123] and [0327]) bits comprise at least some bits received after said start (start, [0088]) sequence.

Referring to claim 34, Yu discloses the system of claim 33 wherein said means for processing in parallel (parallel, [0062]) further comprising means for detecting (detected, [0092]) and end (ending, [0056], [0057], [0107] and [0161]) sequence within said means for storing, after said start (start, [0088]) sequence has been detected (detected, [0092]), during at least one clock cycle subsequent to said first clock cycle (clock cycle, [0227] and [0279]), wherein said valid payload data (payload data, [0123] and [0327]) bits comprise at least some bits received between said start (start, [0088]) and end sequences.

Referring to claim 35, Yu discloses the system of claim 34 further comprising means for detecting an Abort (abort, [0115] and [0134]) sequence contained within said means for storing, during at least one clock cycle subsequent to said first clock cycle

(clock cycle, [0227] and [0279]), wherein if said Abort (abort, [0115] and [0134]) sequence is detected, all bits received after said start sequence are discarded (discard, [0139]) and a search for a new (new, [0176]) start sequence is initiated.

Referring to claim 36, Yu discloses the system of claim 34 further comprising means for detecting at least one stuff (stuff, [0299] and [0300]) bit contained within said means for storing and for discarding (discard, [0139]) said at least one stuff (stuff, [0299] and [0300]) bit, if detected, wherein said valid payload data (payload data, [0123] and [0327]) bits stored in said means for storing after said start sequence and before said end sequence, excluding at least one stuff (stuff, [0299] and [0300]) bit.

Allowable Subject Matter

5. Claims 1-15 are allowed.

6. Claims 23, 24, 29 and 30 are objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.

Conclusion

7. **Any response to this action should be mailed to:**

Commissioner of Patents and Trademarks
Washington, D.C. 20231

or faxed to:

(571) 273-8300, (for formal communications intended for entry)

8. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Jamal A. Fox whose telephone number is (571) 272-3143. The examiner can normally be reached on Monday-Friday 6:30 AM - 5:00 PM.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Wellington Chin can be reached on (571) 272-3134. The fax phone number for the organization where this application or proceeding is assigned is (571) 273-8300.

Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to 2600 Customer Service whose telephone number is (571) 272-2600.

Jamal A. Fox

Jamal A. Fox

WELLINGTON CHIN
SUPERVISORY PATENT EXAMINER